

ABSTRACT OF THE DISCLOSURE

A plurality of memory cell arrays are provided. Each of the memory cell arrays has a plurality of memory cells and the memory cells are connected to a plurality of word lines. Corresponding with the plurality of memory cell arrays, a plurality of word line drive circuits and a plurality of bit line control circuits are provided. Each of the word line drive circuits selects and drives the word lines of the corresponding memory cell array. Each of the bit control circuits carries out verifying reading for the data written in advance in the plurality of memory cells of the corresponding memory cell array, and controls a select and driving operation for the word lines of the corresponding word line drive circuit based on a result of the verifying reading.

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